



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,332	07/22/2003	David R. Hembree	3592.8US (97-0321.08/US)	6977
24247	7590	09/07/2005	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			LEE, CHEUNG	
			ART UNIT	PAPER NUMBER
			2812	
DATE MAILED: 09/07/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/624,332

Applicant(s)

HEMBREE, DAVID R.

Examiner

Cheung Lee

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 February 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 6/17/05
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Notice to Applicant

1. Applicant's Amendment filed on February 18, 2005 has been entered and made of record.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on June 17, 2005, and February 14, 2005 were filed before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desai et al. (U.S. Patent 6,166,434; hereinafter "Desai") in view of Toy et al. (U.S. Patent 6,451,155; hereinafter "Toy").
4. With respect to claims 1, 3, and 5, Desai discloses a method for assembling a Chip On Board semiconductor device on a substrate, said Chip On Board semiconductor device (fig. 2E) having a semiconductor die (fig. 2E, item 200; col. 5,

Art Unit: 2812

lines 38-42) and a heat sink cap (fig. 2E, item 210; col. 5, lines 43-59) abutting a portion of a top surface of a substrate (fig. 2E; col. 6, lines 15-38) including: providing an adhesive between a portion of an upper surface of the semiconductor die and a portion of a lower surface of the heat sink cap (col. 6, lines 43-59) for engaging the semiconductor die and heat sink cap (col. 6, lines 43-59; col. 4, lines 12-34) for abutting the edge of the heat sink cap to the substrate (col. 6, lines 43-59; fig. 2E, items 206 and 210); and placing an encapsulant into the heat sink cap for engaging interior portions of the heat sink cap (fig. 2E, item 208), portions of the semiconductor die (col. 7, lines 1-10), portions of the top surface of the substrate and portions of the adhesive (col. 6, lines 60-67; col. 7, lines 1-10). Desai discloses the two sides 214 and 216 of the clip in figure 2B closely engage two edges of the die when the clip is placed over the die (col. 5, lines 60-67). So, the encapsulant engages portions of the adhesive when an underfill material is dispensed into the gap (fig. 2D, item 207) since there is a gap between the clip and the die. But Desai does not disclose expressly that the adhesive is a compliant adhesive-filled gel silicone elastomer.

Toy discloses a silicon-containing polymeric adhesive (e.g., a silicone elastomeric material) being used to attach a heat sink to the multi-chip module (col. 4, lines 26-40). The examiner interpreted that the silicon-containing polymeric adhesive is compliant since the flexibility of the elastomer can be adjusted by manipulating the relative amount of filler (col. 9, lines 49-67; col. 10, lines 1-6). Besides, the steps of engaging the semiconductor die and the heat sink cap in compliant removable adhesion is achieved before the adhesive is fully cured. And it is obvious to apply any form of

pressure to the semiconductor die into the cap to engage the semiconductor die and the cap.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the adhesive silicone elastomer film as an adhesive between the clip and the semiconductor die. The motivation for doing so would have been to achieve a remarkable heat resistance.

5. With respect to claims 2, 4, and 6, Desai in view of Toy discloses a method for assembling a Chip On Board semiconductor device on a substrate as set forth in claims 1, 3, and 5, Toy discloses wherein the compliant adhesive-filled gel silicone elastomer includes a cross-linked silicone (col. 9, lines 27-48).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2812

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

September 2, 2005



**HANGUYEN
PRIMARY EXAMINER**